RD74LVC374B

Octal D-type Flip Flops with 3-state Outputs

REJ03D0382–0100
Rev.1.00
Nov. 26, 2004

Description

The RD74LVC374B has eight edge trigger D type flip flops with three state outputs in a 20 pin package. Data at the D inputs meeting set up requirements are transferred to the Q outputs on positive going transitions of the clock input. When the clock input goes low, data at the D inputs will be retained at the outputs until clock input returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements. Low voltage and high-speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- V_{CC} = 1.65 V to 5.5 V
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- All outputs V_{OUT} (Max.) = 5.5 V (@V_{CC} = 0 V or output off state)
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25 °C)
- Typical V_{OH} undershoot > 2.0 V (@V_{CC} = 3.3 V, Ta = 25°C)
- High output current ±4 mA (@V_{CC} = 1.65 V)
  ±8 mA (@V_{CC} = 2.3 V)
  ±12 mA (@V_{CC} = 2.7 V)
  ±24 mA (@V_{CC} = 3.0 V to 5.5 V)
- Ordering Information

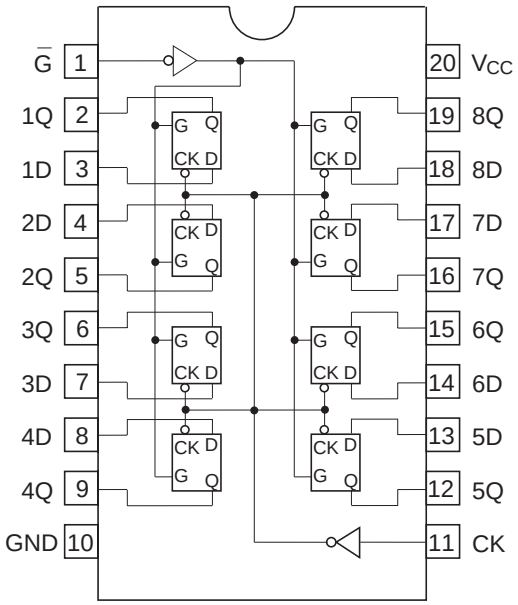
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
RD74LVC374BFPEL	SOP–20 pin (JEITA)	FP–20DAV	FP	EL (2,000 pcs/reel)
RD74LVC374BTELL	TSSOP–20 pin	TTP–20DAV	T	ELL (2,000 pcs/reel)

Function Table

Inputs			Output Q
$\overline{G}$	CK	D	
H	X	X	Z
L	↑	L	L
L	↑	H	H
L	L	X	Q_0

H: High level
L: Low level
X: Immaterial
Z: High impedance
↑: Low to high transition
Q_0: Level of Q before the indicated steady input conditions were established.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.5 to 7.0	V	
Input diode current	I_{IK}	–50	mA	V_I = –0.5 V
Input voltage	V_I	–0.5 to 7.0	V	
Output diode current	I_{OK}	–50	mA	V_O = –0.5 V
		50		V_O = V_{CC}+0.5 V
Output voltage	V_O	–0.5 to V_{CC} +0.5	V	Output "H" or "L"
		–0.5 to 7.0		Output "Z" or V_{CC}:OFF
Output current	I_O	±50	mA	
V_{CC}, GND current / pin	I_{CC} or I_{GND}	100	mA	
Storage temperature	Tstg	–65 to +150	°C	

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	1.5 to 5.5	V	Data hold
		1.65 to 5.5		At operation
Input / output voltage	V_I	0 to 5.5	V	$\overline{G}$, CK, D
	V_O	0 to V_{CC}		Output "H" or "L"
		0 to 5.5		Output "Z" or V_{CC}:OFF
Operating temperature	Ta	–40 to 85	°C	
Output current	I_{OH}	–4	mA	V_{CC} = 1.65 V
		–8		V_{CC} = 2.3 V
		–12		V_{CC} = 2.7 V
		–24		V_{CC} = 3.0 V to 5.5 V
	I_{OL}	4	mA	V_{CC} = 1.65 V
		8		V_{CC} = 2.3 V
		12		V_{CC} = 2.7 V
		24		V_{CC} = 3.0 V to 5.5 V
Input rise / fall time [*1]	t_r, t_f	20	ns/V	V_{CC} = 1.65 V to 2.7 V
		10		V_{CC} = 3.0 V to 5.5 V

Notes: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

Item	Symbol	V_{CC} (V)	Ta = –40 to 85°C		Unit	Test Conditions
			Min	Max		
Input voltage	V_{IH}	1.65 to 1.95	V_{CC}×0.65	—	V	
		2.3 to 2.7	1.7	—		
		2.7 to 3.6	2.0	—		
		4.5 to 5.5	V_{CC}×0.7	—		
	V_{IL}	1.65 to 1.95	—	V_{CC}×0.35		
		2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
		4.5 to 5.5	—	V_{CC}×0.3		
Output voltage	V_{OH}	1.65 to 5.5	V_{CC}–0.2	—	V	I_{OH} = –100 µA
		1.65	1.2	—		I_{OH} = –4 mA
		2.3	1.7	—		I_{OH} = –8 mA
		2.7	2.2	—		I_{OH} = –12 mA
		3.0	2.4	—		
		3.0	2.2	—		I_{OH} = –24 mA
		4.5	3.8	—		
	V_{OL}	1.65 to 5.5	—	0.2		I_{OL} = 100 µA
		1.65	—	0.45		I_{OL} = 4 mA
		2.3	—	0.7		I_{OL} = 8 mA
		2.7	—	0.4		I_{OL} = 12 mA
		3.0	—	0.55		I_{OL} = 24 mA
		4.5	—	0.55		
Input current	I_{IN}	0 to 5.5	—	±5.0	µA	V_{IN} = 5.5 V or GND
Output leak current	I_{OFF}	0	—	±5.0	µA	V_{IN} / V_{OUT} = 5.5 V
Off state output current	I_{OZ}	2.7 to 5.5	—	±5.0	µA	V_{IN} = V_{CC} or GND V_{OUT} = 5.5 V or GND
Quiescent supply current	I_{CC}	2.7 to 3.6	—	±5.0	µA	V_{IN} = 3.6 to 5.5 V
		2.7 to 5.5	—	5.0	µA	V_{IN} = V_{CC} or GND
	ΔI_{CC}	2.7 to 3.6	—	500	µA	V_{IN} = one input at(V_{CC}–0.6)V, other inputs at V_{CC} or GND

Switching Characteristics

Item	Symbol	V_{CC} (V)	Ta = –40 to 85°C			Unit	From (Input)	To (Output)
			Min	Typ	Max			
Maximum clock frequency	f_{max}	1.8±0.15	—	—	55.0	MHz		
		2.5±0.2	—	—	95.0			
		2.7	—	—	150.0			
		3.3±0.3	—	—	150.0			
		5.0±0.5	—	—	150.0			
Propagation delay time	t_{PLH} t_{PHL}	1.8±0.15	1.0	—	21.6	ns	CK	Q
		2.5±0.2	1.0	—	10.5			
		2.7	1.0	—	8.0			
		3.3±0.3	2.2	—	7.0			
		5.0±0.5	1.0	—	5.5			
Output enable time	t_{ZH} t_{ZL}	1.8±0.15	1.0	—	19.5	ns	$\overline{G}$	Q
		2.5±0.2	1.0	—	10.5			
		2.7	1.0	—	8.5			
		3.3±0.3	1.5	—	7.5			
		5.0±0.5	1.0	—	5.5			
Output disable time	t_{HZ} t_{LZ}	1.8±0.15	1.0	—	18.8	ns	$\overline{G}$	Q
		2.5±0.2	1.0	—	7.8			
		2.7	1.0	—	7.0			
		3.3±0.3	1.7	—	6.4			
		5.0±0.5	1.0	—	5.4			
Setup time	t_{su}	1.8±0.15	6.0	—	—	ns		
		2.5±0.2	4.0	—	—			
		2.7	2.0	—	—			
		3.3±0.3	2.0	—	—			
		5.0±0.5	2.0	—	—			
Hold time	t_h	1.8±0.15	4.0	—	—	ns		
		2.5±0.2	2.0	—	—			
		2.7	1.5	—	—			
		3.3±0.3	1.5	—	—			
		5.0±0.5	1.5	—	—			
Pulse width	t_w	1.8±0.15	9.0	—	—	ns		
		2.5±0.2	4.0	—	—			
		2.7	3.3	—	—			
		3.3±0.3	3.3	—	—			
		5.0±0.5	3.3	—	—			
Between output pins skew[*1]	t_{OSLH} t_{OSHL}	1.8±0.15	—	—	—	ns		
		2.5±0.2	—	—	—			
		2.7	—	—	—			
		3.3±0.3	—	—	1.0			
		5.0±0.5	—	—	1.0			
Input capacitance	C_{IN}	3.3	—	4.0	—	pF		
Output capacitance	C_O	3.3	—	8.0	—	pF		

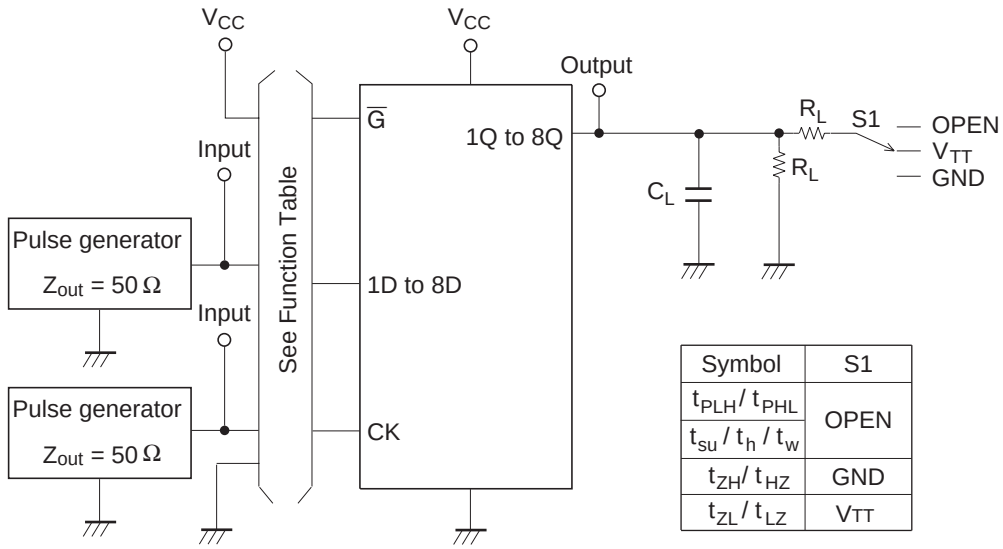
Note: 1. This parameter is characterized but not tested.

$tos_{LH} = | t_{PLHm} - t_{PLHn} |$, $tos_{HL} = | t_{PHLm} - t_{PHLn} |$

Operating Characteristics

Item	Symbol	V_{CC} (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C_{PD}	1.8	—	25	—	pF	f = 10 MHz
		2.5	—	26	—		
		3.3	—	28	—		
		5.0	—	32	—		

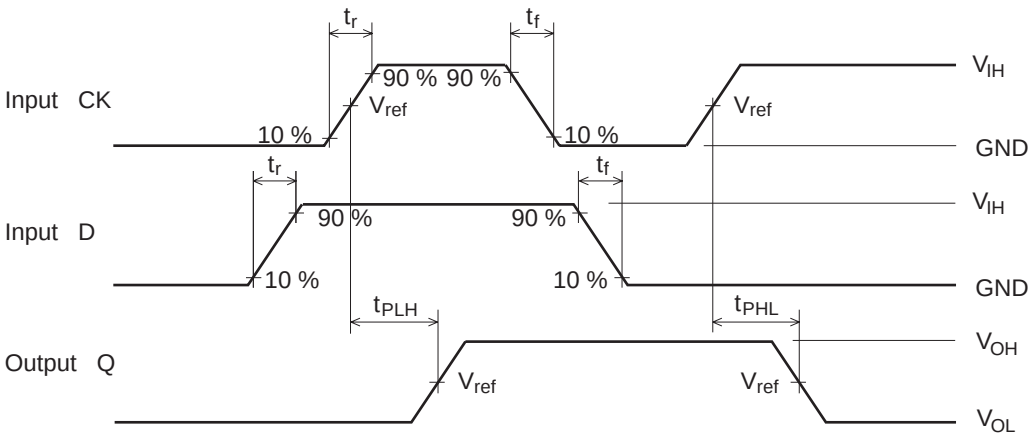
Test Circuit



Symbol	S1
t_{PLH} / t_{PHL}	OPEN
t_{su} / t_h / t_w	
t_{ZH} / t_{HZ}	GND
t_{ZL} / t_{LZ}	VTT

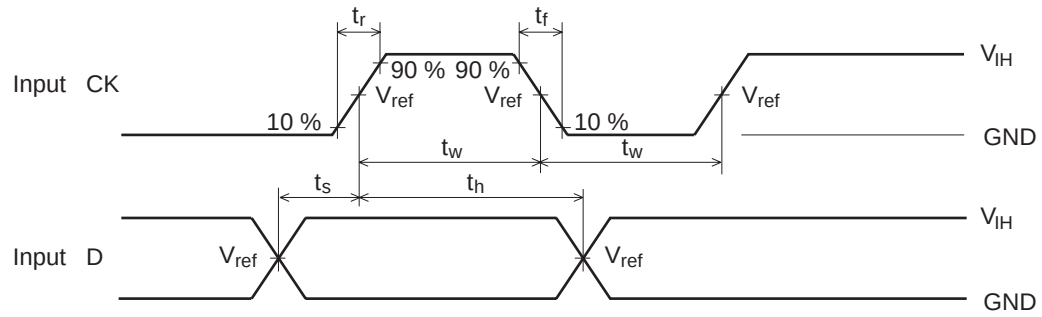
Note: 1. C_L includes probe and jig capacitance.

Waveforms – 1



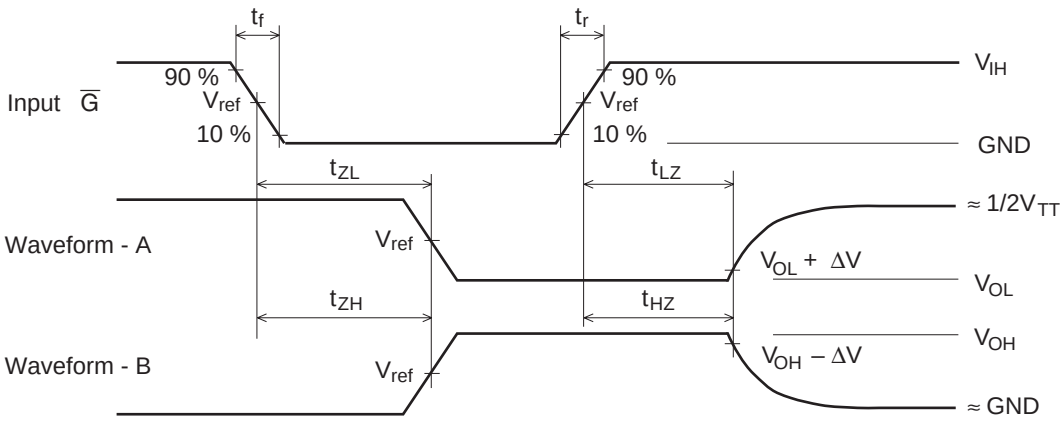
Note: Input waveform: PRR = 10 MHz, duty cycle 50%.

Waveforms – 2



Note: Input waveform: PRR = 10 MHz, duty cycle 50%.

Waveforms – 3



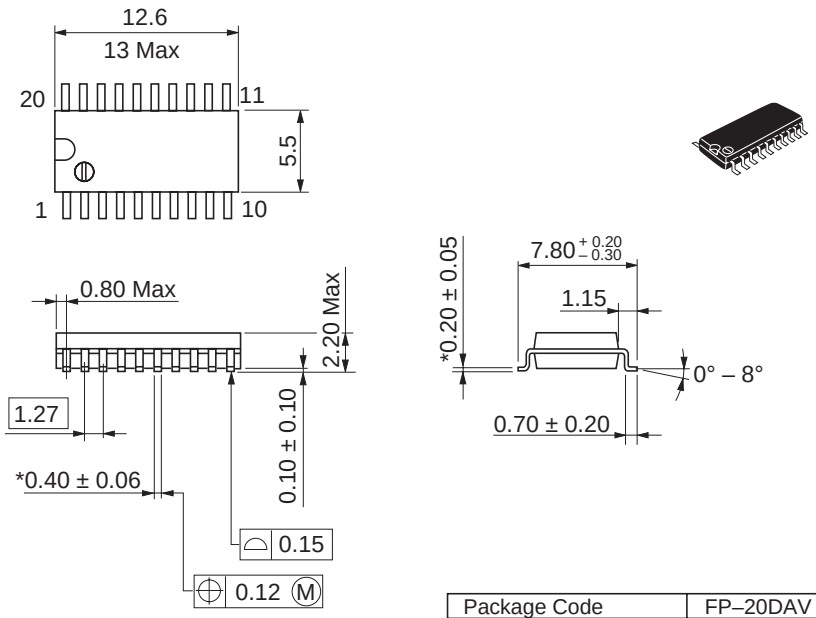
V_{CC} (V)	INPUTS		Vref	V_{TT}	C_L	R_L	ΔV
	V_{IH}	t_r/t_f					
V_{CC} = 1.8±0.15 V	V_{CC}	≤ 2 ns	1/2 V_{CC}	2× V_{CC}	30 pF	1.0 kΩ	0.15 V
V_{CC} = 2.5±0.2 V	V_{CC}	≤ 2 ns	1/2 V_{CC}	2× V_{CC}	30 pF	500 Ω	0.15 V
V_{CC} = 2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
V_{CC} = 3.3±0.3 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
V_{CC} = 5.0±0.5 V	V_{CC}	≤ 2.5 ns	1/2 V_{CC}	2× V_{CC}	50 pF	500 Ω	0.3 V

Notes:
1. Input waveform : PRR = 10 MHz, duty cycle 50%.
2. Waveform – A shows input conditions such that the output is "L" level when enable by the output control.
3. Waveform – B shows input conditions such that the output is "H" level when enable by the output control.

Package Dimensions

As of January, 2003

Unit: mm

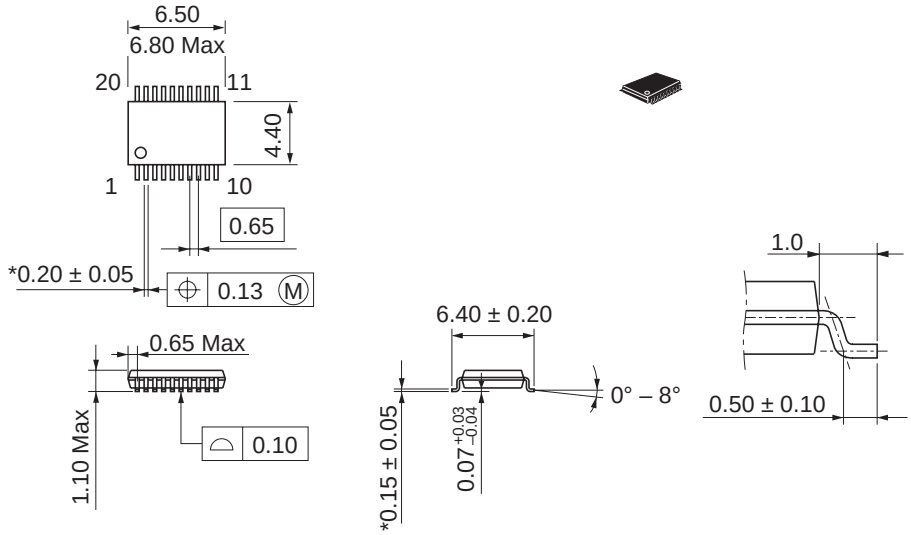


*Pd plating

Package Code	FP–20DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.31 g

As of January, 2003

Unit: mm



*Pd plating

Package Code	TTP–20DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.07 g

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Colophon .2.0